

MAC4DLM

Preferred Device

Sensitive Gate Triacs

Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Four-Quadrant Triggering
- Blocking Voltage to 600 V
- On-State Current Rating of 4.0 Amperes RMS at 93°C
- Low Level Triggering and Holding Characteristics
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60 Hz, Gate Open)	V_{DRM} , V_{RRM}	600	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, $T_C = 93^\circ\text{C}$)	$I_{\text{T(RMS)}}$	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, $T_J = 110^\circ\text{C}$)	I_{TSM}	40	A
Circuit Fusing Consideration ($t = 8.3$ msec)	I^2t	6.6	A^2sec
Peak Gate Power (Pulse Width ≤ 10 μsec , $T_C = 93^\circ\text{C}$)	P_{GM}	2.0	W
Average Gate Power ($t = 8.3$ msec, $T_C = 93^\circ\text{C}$)	$P_{\text{G(AV)}}$	1.0	W
Peak Gate Current (Pulse Width ≤ 20 μsec , $T_C = 93^\circ\text{C}$)	I_{GM}	4.0	A
Peak Gate Voltage (Pulse Width ≤ 20 μsec , $T_C = 93^\circ\text{C}$)	V_{GM}	5.0	V
Operating Junction Temperature Range	T_J	-40 to 110	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

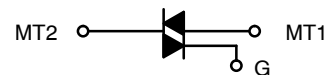
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



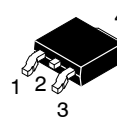
ON Semiconductor®

<http://onsemi.com>

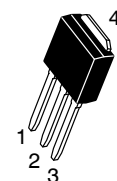
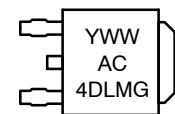
TRIACS 4.0 AMPERES RMS 600 – 800 VOLTS



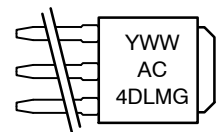
MARKING DIAGRAMS



**DPAK
CASE 369C
STYLE 6**



**DPAK-3
CASE 369D
STYLE 6**



Y = Year
WW = Work Week
AC4DLM = Device Code
G = Pb-Free Package

PIN ASSIGNMENT

1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

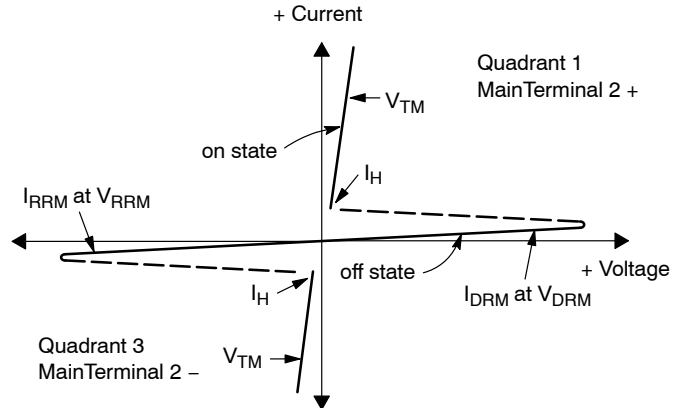
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

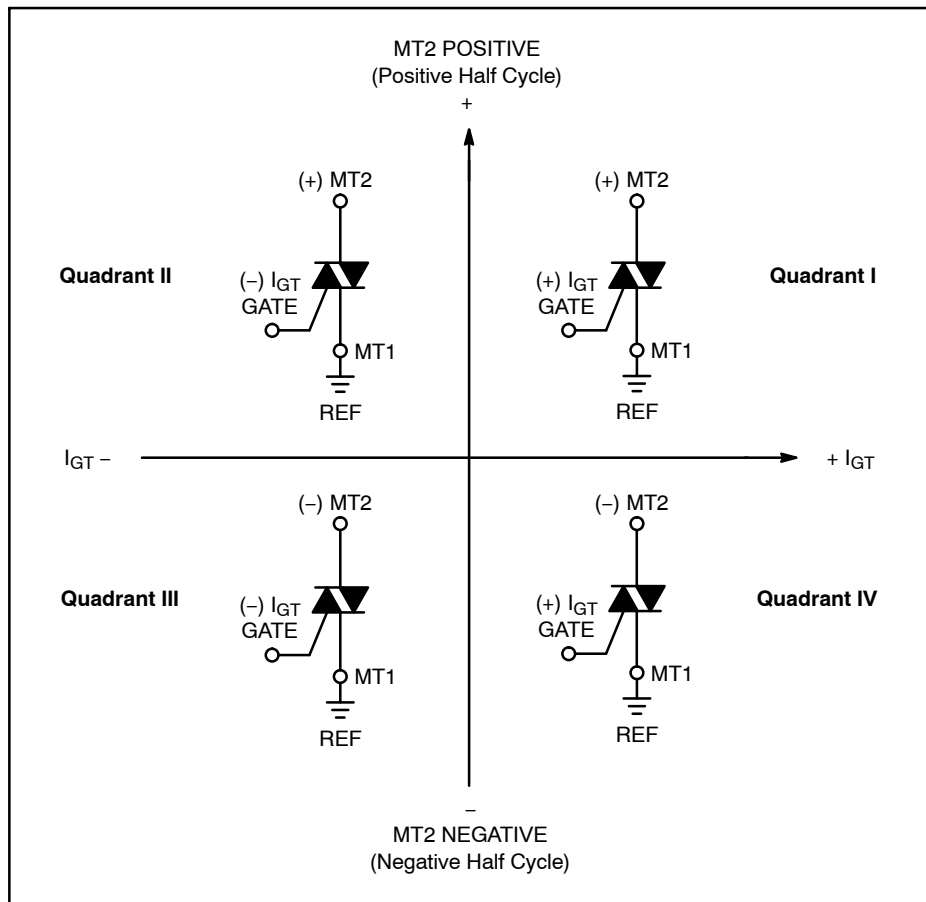
MAC4DLM

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off-State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off-State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On-State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

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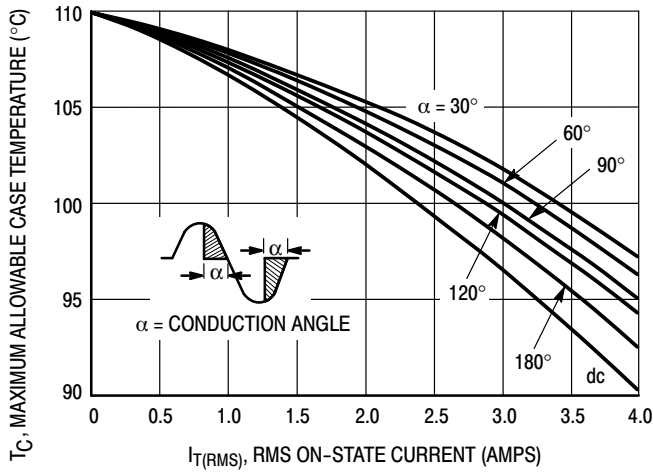


Figure 1. RMS Current Derating

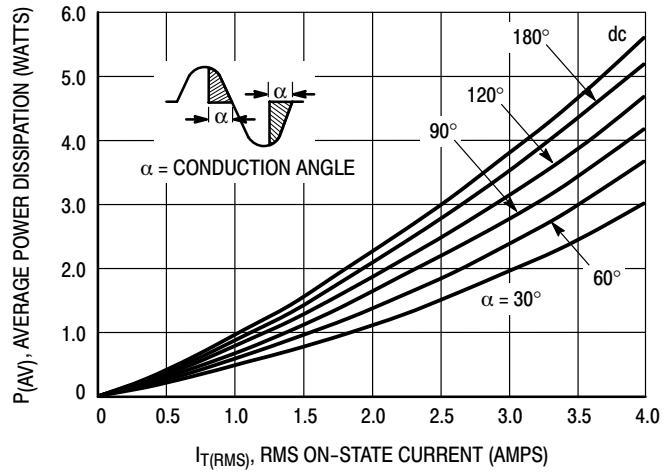


Figure 2. On-State Power Dissipation

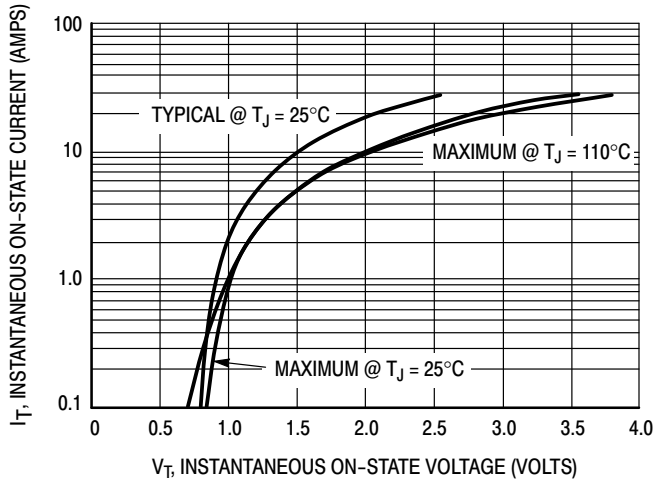


Figure 3. On-State Characteristics

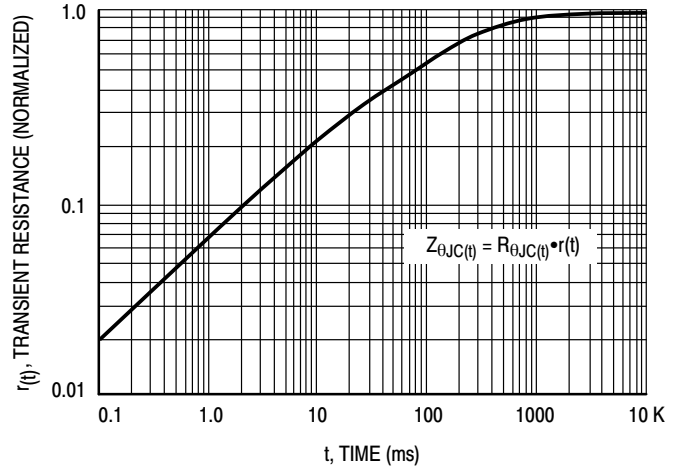


Figure 4. Transient Thermal Response

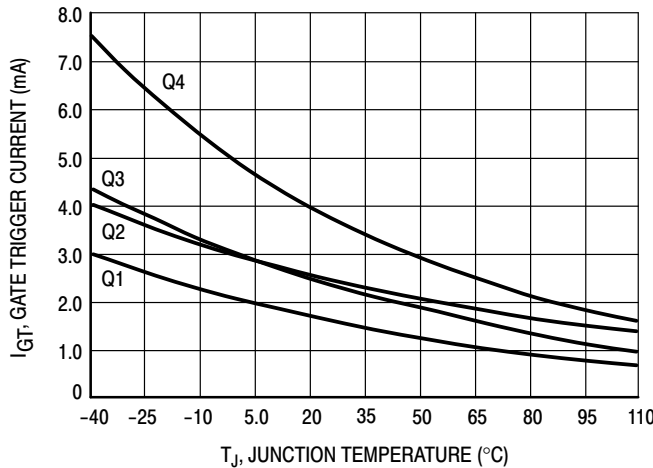


Figure 5. Typical Gate Trigger Current versus Junction Temperature

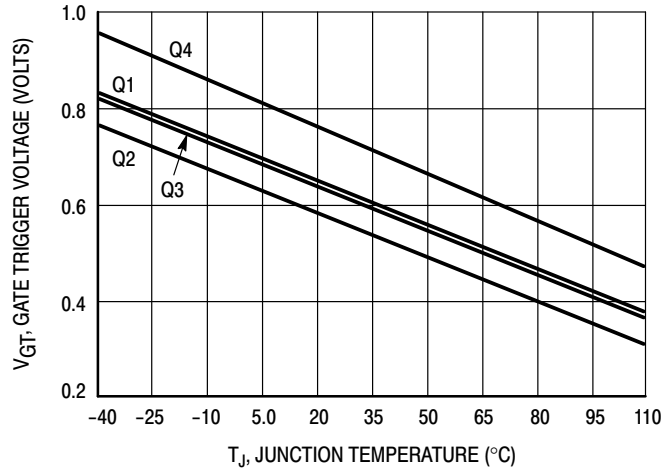


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

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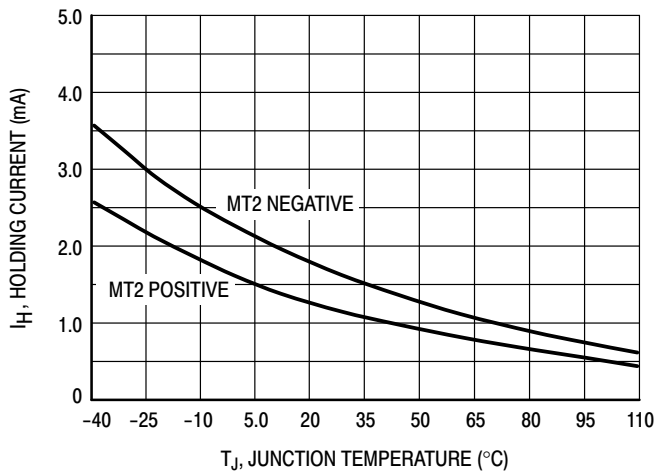


Figure 7. Typical Holding Current versus Junction Temperature

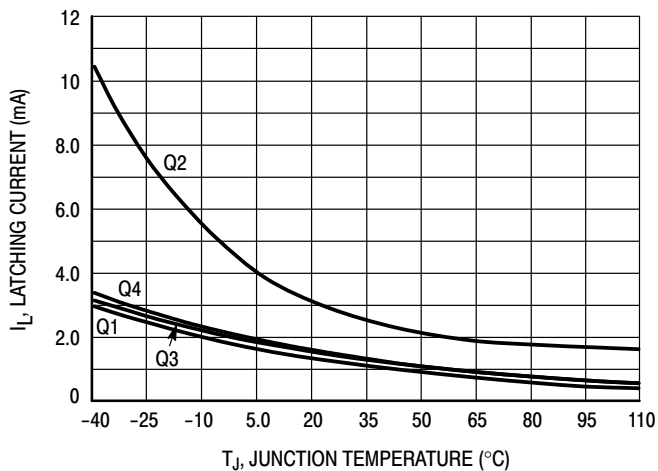


Figure 8. Typical Latching Current versus Junction Temperature

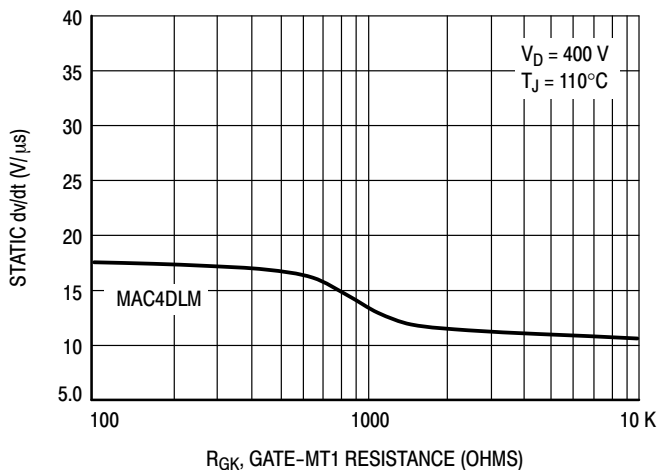


Figure 9. Minimum Exponential Static dv/dt versus Gate-MT1 Resistance

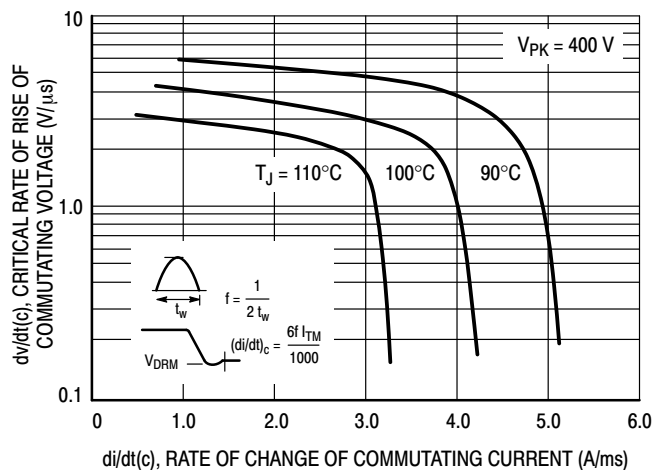
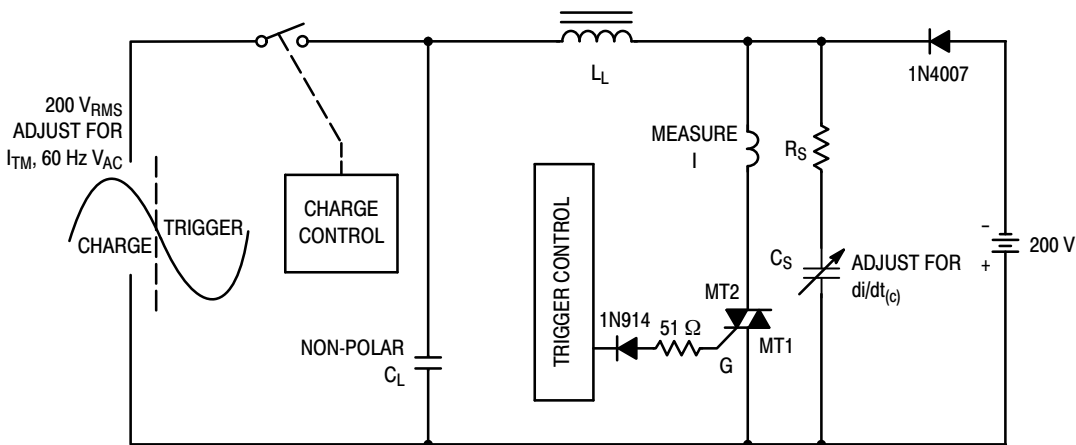


Figure 10. Critical Rate of Rise of Commutating Voltage



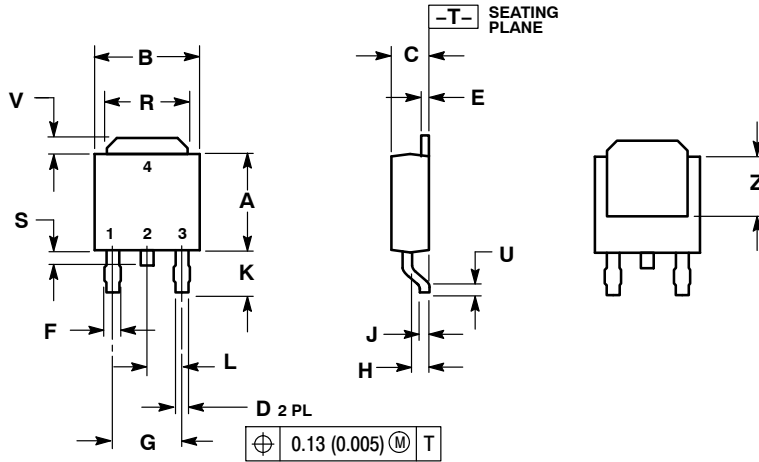
Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

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PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

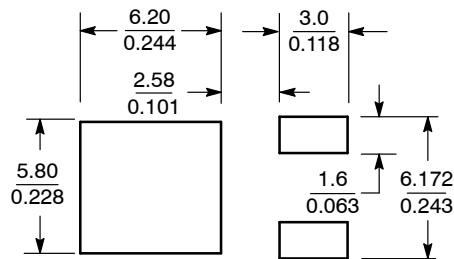


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

SOLDERING FOOTPRINT*



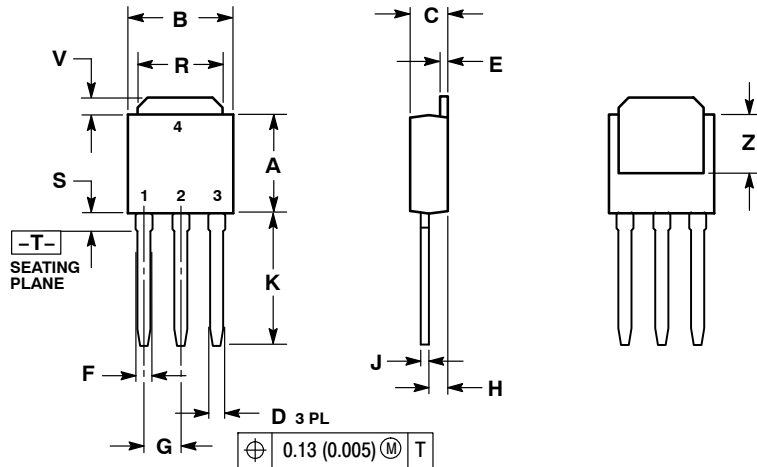
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAC4DLM

PACKAGE DIMENSIONS

DKPAK-3
CASE 369D-01
ISSUE B




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:

- PIN 1. MT1
- MT2
- GATE
- MT2

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